

Abstract

A test mode circuit of a semiconductor memory device features a test mode controller, a test mode decoder and a test mode item selecting means. The test mode controller outputs a test mode setting signal to control a test mode setting operation in response to a register set signal and address signals which are used in setting a test mode. The test mode decoder, which is controlled by the test mode setting signal, selects a test mode item group in response to upper address bits of the address signal. The particular test mode is then selected from the test mode group in response to lower address bits of the address signal. Accordingly, the number of metal lines used in a test mode circuit can be reduced.